IOANNIS SAVIDIS

35 Noel Drive • Rochester, NY 14606
Phone: (585) 426-2127 • Cell: (585) 737-7916
ioannis.savidis@rochester.edu
U.S Citizen

RESEARCH AND TEACHING INTERESTS

- Large scale digital, analog, and mixed-signal integrated circuits, containing RF transmitters, sensors, analog-to-digital converters, and high speed digital cores.
- Modeling and analysis of complex structures such as on-chip interconnects, power/clock distribution networks, and the monolithic substrate that support these various circuits.
- Circuit level design considerations for emerging technologies such as nanowire and grapheme are of particular interest, focusing on systems level integration with traditional CMOS technology.
- More generally, systems integration of disparate technology, including III-V semiconductors, RF, optics, etc., with 3-D integration or silicon carrier based techniques providing the means to merge these heterogeneous technologies
- 3-D integrated circuits, with an emphasis on electrical and thermal modeling and characterization, signal and power integrity, and power and clock delivery for 3-D stacking technologies.
- Interconnect related issues in 2-D and 3-D integrated circuits
- Power management for SoC and microprocessor circuits
- Implement pedagogical techniques, including effective evidence-based teaching practices, that incorporate learner centered teaching, technology in the classroom (clickers, web based media, etc.), and assessment based learning. Courses of interest include digital VLSI circuit design, mixed signal/analog design, digital logic, and device physics (MOS, BJT, and emerging technologies such as graphene and nano-wires)

EDUCATION

University of Rochester, Rochester, NY; ***Ph.D. Electrical and Computer Engineering***, advised by Prof. Eby G. Friedman., Dissertation titled *Characterization and Modeling of TSV Based 3-D Integrated Circuits,* graduation May 2013.

University of Rochester, Rochester, NY; ***M.S. Electrical and Computer Engineering***, May 2007.
Cumulative GPA: 3.85/4.0

Relevant course work: Semiconductor Devices; Digital Integrated Circuit Design; RF Integrated Circuits; Performance Issues in VLSI/IC; Advanced Analog CMOS Integrated Circuit Design II; Random Processes

Duke University, Durham, NC; *B.S.E. Electrical and Computer Engineering; Biomedical Engineering*, May 2005.
Cumulative GPA: 3.18/4.0; Engineering GPA: 3.44/4.0

Relevant course work: Semiconductor Electronic Devices; Linear Systems; Switch Theory; Computer Architecture; Integrated Circuits; Electromagnetics; Advanced Semiconductor Devices; Full Custom VLSI design; IC design; Program Design/Analysis II, Bioelectricity, Fundamentals of Biomaterials and Biomechanics, Intro to Biomaterials, Biomedical Electronics

Continuing education: Enrolled in Massive Online Open Courses (MOOC) through Coursera, edX, Udacity, and CIRTL

Enrolled in *MOS Transistors* (Prof. Yannis Tsividis, Columbia University), *VLSI CAD: Logic to Layout* (Prof. Rob Rutenbar, Unversity of Illinois at Urbana-Champaign), *The College Classroom* (Profs. Peter Newbury and Elizabeth Simon, University of California San Diego)

RESEARCH – AWARDS/PUBLICATIONS/GRANTS

Awards

IEEE International Symposium on Circuits and Systems (ISCAS '08) Best Paper Award Finalist; paper [13] was selected as one of ten papers for a special poster session competing for the Best Paper Award.

IEEE Southeast Regional Top 10 Paper Finalist; paper [13] was selected as one of ten papers that was then presented at IEEE SoutheastCon 2004.

University of Rochester Dean's Fellowship, two-year, merit based fellowship, University of Rochester, Sept. 2005 – May 2007.

Duke University Pratt Fellows Program; one and a half year engineering fellowship, Duke University, January 2004 – May 2005.

Publications

Total Citaton Count of 190+, excluding self-citations. h-index of 6

Book Chapters

[1] I. Savidis and E. G. Friedman, "Physical Design Trends for Interconnects," *On-Chip Communication Architectures System on Chip Interconnect*, S. Pasricha and N. Dutt, Morgan Kaufmann Publishers, Elsevier, Chapter 11, pp. 403-437, 2008, ISBN # 978-0-12-373892-9.

Journal Papers

[1] I. Savidis, S. Kose, and E. G. Friedman, "Power Noise in TSV-Based 3-D Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 48, No. 2, February 2013.

[2] B. Ciftcioglu, J. Xue, A. Garg, R. Berman, J. Hu, S. Wang, M. Jain, I. Savidis, P. Liu, M. Huang, E. G. Friedman, D. Moore, G. Wicks, and H. Wu, "A 3-D Integrated Intra-chip Free-Space Optical Interconnect for Multi-Core Processors," *submitted to IEEE Journal of Emerging and Selected Topics in Circuits and Systems (JESTCS'12).*

[3] B. Ciftcioglu, R. Berman, S. Wang, J. Hu, I. Savidis, M. Jain, D. Moore, M. Huang, E. G. Friedman, G. Wicks, and H. Wu, "3-D Integrated Heterogeneous Intra-Chip Free-Space Optical Interconnect," *Optics Express*, Vol. 20, No. 4, pp. 4331-4345, February 2012.

[4] V. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks in 3-D Integrated Systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 12, pp. 2256-2266, December 2011.

[5] J. Wang, I. Savidis, and E. G. Friedman, "Thermal Analysis of Oxide-Confined VCSEL Arrays," *Microelectronics Journal*, Vol. 42, No. 5, pp. 820-825, May 2011.

[6] B. Ciftcioglu, R. Berman, J. Zhang, Z. Darling, S. Wang, J. Hu, J. Xue, A. Garg, M. Jain, I. Savidis, D. Moore, M. Huang, E. G. Friedman, G. Wicks, and H. Wu, "A 3-D Integrated Intra-Chip Free-Space Optical Interconnect for Many-Core Chips," *IEEE Photonics Technology Letters*, Vol. 23, No. 3, pp. 164-166, February 2011.

[7] I. Savidis, S. M. Alam, A. Jain, S. Pozder, R. E. Jones, and R. Chatterjee, "Electrical Modeling and Characterization of Through-Silicon vias (TSVs) for 3-D Integrated Circuits," *Microelectronics Journal*, Vol. 41, No. 1, pp. 9-16, January 2010.

[8] I. Savidis and E. G. Friedman, "Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Transactions on Electron Devices*, Vol. 56, No. 9, pp. 1873-1881, September 2009.

Conference Papers

[1] I. Savidis and E. G. Friedman, "Test Circuits for 3-D Systems Integration," *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, pp. 181-184, March 2012.

[2] H. Wu, B. Ciftcioglu, R. Berman, S. Wang, J. Hu, I. Savidis, M. Jain, D. Moore, M. Huang, E. Friedman, and G. Wicks, "Chip-Scale Demonstration of 3-D Integrated Intra-Chip Free-Space Optical Interconnect (Invited Paper)," *Photonics West: SPIE Optoelectronic Integrated Circuits XIV,* Feb. 2012.

[3] I. Savidis, V. Pavlidis, and E. G. Friedman, "Clock Distribution Models of 3-D Integrated Systems," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2225-2228 May 2011.

[4] I. Savidis, S. Kose, and E. G. Friedman, "Power Grid Noise in TSV-Based 3-D Integrated Systems," *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, pp. 129-132, March 2011.

[5] B. Ciftcioglu, R. Berman, J. Zhang, Z. Darling, A. Garg, J. Hu, M. Jain, P. Liu, I. Savidis, S. Wang, J. Xue, E. G Friedman, M. Huang, D. Moore, G. Wicks, and H. Wu, "Initial Results of Prototyping a 3-D Integrated Intra-Chip Free-Space Optical Interconnect," *Proceedings of the Workshop on the Interaction between Nanophotonic Devices and Systems (WINDS 2010)*, December 2010.

[6] J. Xue, A. Garg, B. Ciftcioglu, J. Hu, S. Wang, I. Savidis, M. Jain, R. Berman, P. Liu, M. Huang, H. Wu, E. Friedman, G. Wicks, and D. Moore, "An Intra-Chip Free-Space Optical Interconnect," *ISCA '10: Proceedings of the 37th Annual International Symposium on Computer Architecture*, pp. 94-105, June 2010.

[7] B. Ciftcioglu, R. Berman, J. Zhang, Z. Darling, S. Wang, J. Hu, J. Xue, A. Garg, M. Jain, I. Savidis, D. Moore, M. Huang, E. G Friedman, G. Wicks, and H. Wu, "3-D Integrated Intra-Chip Free-Space Optical Interconnect", 2010 IEEE International Solid-State Circuits Conference (ISSCC) Student Research Forum, February 2010.

[8] J. Xue, A. Garg, B. Ciftcioglu, S. Wang, I. Savidis, J. Hu, M. Jain, M. Huang, H. Wu, E. G. Friedman, G. W. Wicks, and D. Moore, "An Intra-Chip Free-Space Optical Interconnect," *Proceedings of the 3rd Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI '09) held in conjunction with the 36th International Symposium on*

Computer Architecture, June 2009.

[9] I. Savidis, E. G. Friedman, V. F. Pavlidis, and G. De Micheli, "Clock and Power Distribution Networks for 3-D Integrated Circuits," *Proceedings of the Workshop on 3D Integration, Design, Automation & Test in Europe Conference,* March 2009.

[10] I. Savidis, S. M. Alam, A. Jain, S. Pozder, R. E. Jones, and R. Chatterjee, "Electrical Modeling and Characterization of Through-Silicon vias (TSVs) for 3-D Integrated Circuits," *Proceedings of VLSI/ULSI Multilevel Interconnect Conference (VMIC)*, pp. 181-186, Oct. 2008.

[11] V. F. Pavlidis, I. Savidis, E. G. Friedman, "Clock Distribution Architectures for 3-D SOI Integrated Circuits," *Proceedings of the IEEE International SOI Conference,* pp. 111-112, October 2008.

[12] V. F. Pavlidis, I. Savidis, E. G. Friedman, "Clock Distribution Networks for 3-D Integrated Circuits," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 651-654, September 2008.

[13] I. Savidis and Eby G. Friedman, "Electrical Modeling and Characterization of 3-D Vias," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 784-787, May 2008.

[14] I. Savidis, A. Jukna, and R. Sobolewski, "Contactless Determination of T_c in Very Small Single Crystal MgB_2 and Thin Film YBCO," *IEEE Student Paper Contest SoutheastCon 2004*, March 2004.

[15] I. Savidis, and R. Sobolewski, "Characterization of Josephson Junctions," *University of Rochester Journal*, August 2000.

Workshop Presentations

[1] I. Vaisband, S. Kose, I. Savidis, and E. G. Friedman, "On-Chip Power Delivery," CEIS University Technology Showcase, Rochester, New York, April 6, 2011.

[2] I. Savidis and E. G. Friedman, "Clock Distribution Topologies for 3-D Integrated Circuits," CEIS University Technology Showcase, Rochester, New York, February 12, 2009.

[3] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks for 3-D Integrated Circuits," Massachusetts Institute of Technology Lincoln Laboratory's 3-D Integrated Circuit Multi-Project Wafer Review, Boston, Massachusetts, September 15, 2008.

[4] I. Savidis and E. G. Friedman, "Electrical Modeling and Characterization of 3-D Vias," *IEEE International Symposium on Circuits and Systems (ISCAS) Best Paper Award Contest*, May 2008.

Conference Presenter

[1] Presented "Clock Distribution Models of 3-D Integrated Systems," at the *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2011.

[2] Presented "Power Grid Noise in TSV-Based 3-D Integrated Systems," at the *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, March 2011.

[3] Presented "Clock Distribution and Power Delivery for 3-D Integrated Circuits," at the *Integrated Circuit Design Meeting* (internal), January 2009.

[4] Presented "Clock Distribution Architectures for 3-D SOI Integrated Circuits," at the *IEEE International SOI Conference,* pp. 111-112, October 2008.

[5] Presented "Electrical Modeling and Characterization of 3-D Vias," at the *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2008.

[6] Presented "Clock and Power Distribution Networks for Three-Dimensional Circuits: Preliminary Design Review," at the *Integrated Circuits Design Meeting* (internal), October 2006.

[7] Presented "Contactless Determination of T_c in Very Small Single Crystal MgB_2 and Thin Film YBCO," at the *IEEE Student Paper Contest SoutheastCon 2004*, March 2004.

Significantly contributed in the development of presentations for Government Agencies:

National Science Foundation (NSF), "Recent Research in 3-D Circuit Design and Related Test Circuits," March 2011.

National Science Foundation, "MOS Current Mode Logic for Low Power Circuits," November 2011.

National Security Agency (NSA), "Recent Research in 3-D Power Delivery," October 2010.

Significantly contributed in the development of presentations for universities and conferences:

Technion Israeli Institute of Technology, "Recent Research in 3-D Circuit Design and Related Test Circuits," March 2012.

2nd Design for 3-D Silicon Integration Workshop, "3-D Design: Architectures, Methodologies, and Test Circuits," May 2010.

Design, Automation & Test in Europe (DATE), "Clock and Power Distribution Networks for 3-D Integrated Circuits," April 2009.

Technion Israeli Institute of Technology, "Electrical Modeling and Characterization of 3-D Vias," February 2009.

2nd Workshop on Diagnostic Services in Network-on-Chips – Test, Debug, and On-Line Monitoring, "Physical Design Issues and Technology Trends in Networks-on-Chip," June 2008.

Technical Industrial Presentations

[1] Presented various bi-weekly update reports to Cisco Systems, Inc. for "3-D Test Circuit on Power Delivery," Award number: 056165-002, 06/2012 – 08/2012.

[2] Presented "Recent Research in 3-D Circuit Design and Related Test Circuits," to Qualcomm Research October 2011.

[3] Presented "Recent Research in 3-D Circuit Design and Related Test Circuits," to Samsung Research September 2011.

[4] Presented "Lessons Learned in 3-D Verification," to Kodak Research, Kodak Park, Rochester, NY, October 2008.

Significantly contributed in the development of presentations:

Samsung, "Power Delivery in Heterogeneous Integrated Circuits," May 2012.

SEMATECH, "Optical Interconnect, Integrated Photonics, and 3-D Packaging," October 2011.

Grants

Significantly contributed in the writing of grants for government granting agencies:

Office of Naval Research (ONR) and Department of Defense (DoD) Multidisciplinary University Research Initiative (MURI) – "Advanced Heterogeneous 3-D Systems Integration: Merging High Speed Nanowire Devices with CMOS".

National Science Foundation (NSF): Collaborative (5 groups) multi-million dollar project titled "3D-Integrated Intra-Chip Free-Space Optical Interconnect for Future Multi-Core SoCs".

Defense Advanced Research Projects Agency (DARPA), "Energy Efficient Systems: 3-D Integration, Advanced Circuits, and Architecture".

Significantly contributed in the writing of grants for industrial partnerships:

Cisco Systems, Inc – "3-D Test Circuit on Power Delivery".

Tezzaron Semiconductor – DARPA sponsored fabrication run (3-D IC) for, "Synchronization, Power Delivery, and 3-D Memory/Logic Architectures," 2009.

Massachusetts Institute of Technology Lincoln Laboratory (MITLL) – DARPA sponsored fabrication run (3-D IC) for, "Noise Propagation in TSV-Based 3-D Integrated Circuits," 2008.

Also submitted to Intel, Qualcomm, Semiconductor Research Corporation (SRC), and Sematech.

Written numerous annual, semi-annual, and final project reports:

NSF, "3D-Integrated Intra-Chip Free-Space Optical Interconnect for Future Multi-Core SoCs".

NSF, "Design Methodologies and Algorithms for Three-Dimensional Integrated Systems"

Center for Electronic Imaging Systems, Centers for Advanced Technology (CAT), "Hybrid Design Methodologies for High Performance Three-Dimensional Image Sensing System-On-Chip Integrated Circuits"

Center for Electronic Imaging Systems, Centers for Advanced Technology (CAT), "Interconnect, Clock, and Power/Ground Distribution Networks in SoC/3-D Integrated Systems".

RESEARCH EXPERIENCE

- Designed and fabricated test circuits at IBM TJ Watson Research Center (Yorktown Heights, NY) characterizing the 3-D integration fabrication process (through-silicon via yield). Test circuits were also designed to electrically characterize the through-silicon via (TSV), investigate the impact of thermal cycling on the TSV, and examine mismatch losses (insertion, attenuation, reflection, transmission, and return) arising from TSV placement in high frequency signal paths.
- Electromagnetic modeling of the TSV for simulation in Ansoft (now part of Ansys) HFSS or Quick 3-D. Full wave simulations were performed to electrically characterize the TSV will at IBM TJ Watson Research Center (Yorktown Heights, NY). Part of my research included tool development of a Java Script based GUI interface that automates model

creation of TSV structures for HFSS and Quick 3-D simulation.

- System level design and implementation of a 3-D integrated intra-chip free-space optical interconnect system for multi-core communication with a group of five professors and twelve graduate students. Designed and fabricated photodetectors and VCSEL arrays, as well as a 3-D integrated transceiver and computing core. Included, additional test circuits investigating thermal conduction amongst 3-D stacked device planes and impact of on-chip decoupling capacitor placement on noise propagation.
- Developed closed-form expressions of the resistance, inductance, and capacitance of interplane 3-D vias.
- Designed a test chip to characterize ground and power noise on various 3-D power distribution topologies. The test chip was fabricated by MIT's Lincoln Laboratory (the 2nd test chip fabricated by MIT's Lincoln Labs).
- Electrically characterized the *RLC* impedance of interplane vias for 3-D integrated circuits; modeled 3-D via to 3-D via inductive and capacitive coupling noise for various circuit topologies.
- Designed circuitry to examine various clock and power distribution topologies for 3D IC's with another student in a collaborative project with MIT's Lincoln Laboratory; clock distribution schemes implemented in silicon were H-tree, trunk, and ring; power was distributed through grid and periphery topologies.
- Implemented cosine transform function in hardware with team of three; developed schematics and layout for the ~38,000 transistor design using Mentor Graphic's ic and da programs; performed simulations to determine power consumption and overall functionality.
- Performed HSPICE simulations of both a 128x128 DRAM and SRAM cell with sense amplifier circuitry as part of two member group; analyzed power consumption and conducted transient analysis on both circuits.
- Designed (layout and schematic) and simulated a low-powered, pipelined 8-bit Brent-Kung adder in Cadence; performed simulations to determine the peak power consumption, set and hold times, and functionality with transient analysis.
- Designed the phase detector, charge pump, and loop filter of an injection-locked oscillator that included a front end of a receiver with ADS; performed simulations on each block of the design to assure each block met specifications set at the onset of the project.
- Examined low power clock distribution networks through a literature search; focused on identifying means of minimizing power consumption on the clock distribution network; presented results to class.
- Modified the Calibre LVS deck to detect devices not currently included such as via chains and kelvins; developed a general MOSFET definition to detect layers overlaying transistors; combined LVS decks for cmos090nvm, cmos090soi, and cmos090 into a single deck (while at Freescale).

PROFESSIONAL EXPERIENCE

May 2009 – June 2011: **IBM Research**, *Yorktown Heights, NY*

Manager: Dr. John U. Knickerbocker, *Mentors*: Dr. Bucknell C. Webb, Dr. Bing Dang, Mr. Paul S. Andry

Group: System on Package and 3-D Integration

Designed circuits to examine package level integration (die on silicon carrier technology that includes a redistribution level for die to die bi-directional communication) through various test vehicles that include C4 bump chains, interdie C4 bump chains, four-point measurements for C4 bump characterization, 20 to 40 mm long transmission lines, and mechanical tests to determine the minimum spacing permitted between to die bonded to the same silicon carrier.

Designed mask sets characterizing the electrical properties of 3-D vias and microbumps. Designed multi-voltage tap structures (on-chip four point measurements), TSV via chains, connectivity test sites, and other test vehicles to characterize the TSVs.

Involved in design of power and ground distribution networks for Madison Project.

Analyzed DRC, LVS, extraction, and Router tools for potential use in 3-D design flow.

Improved GUI and continued high frequency electrical characterization and modeling of interplane 3-D vias using Ansoft's Quick 3-D and HFSS.

May 2008 – August 2008: **IBM Research**, *Yorktown Heights, NY*

Manager: Dr. John U. Knickerbocker, *Mentor*: Dr. Chirag Patel

Group: System on Package and 3-D Integration

Completed high frequency electrical characterization and modeling of interplane 3-D vias using Ansoft's Quick 3-D and HFSS.

Developed Java interface with Quick 3-D and HFSS to quickly produce models of TSV's for various lengths, diameters, dielectric thickness, via-to-via pitch, and number of surrounding vias for electrical simulation.

May 2007 – August 2007: **Freescale Semiconductor**, *Austin, TX*

Manager: Dr. Robert E. Jones, *Mentor:* Dr. Ankur Jain, Dr. Ritwik Chatterjee

Performed electrical characterization and modeling of interplane 3-D vias.

System level HSPICE simulations of global interconnects for both 2-D and 3-D chip configurations.

May 2006 – August 2006: **Freescale Semiconductor**, *Austin, TX*

Manager: Dr. Brad Smith, *Mentor:* Dr. Douglas Reber

Modified the Calibre LVS deck to detect via chains and kelvins (modifying SVRF scripts).

Added general MOSFET definition to Calibre LVS deck (with SVRF language).

Combined cmos090nvm, cmos090soi, and cmos090 into a single LVS deck.

September 2006 – Present: **University of Rochester Graduate Research Assistant (RA)**, *Rochester, NY*

Advised by: Prof. Eby G. Friedman

Member of the *High Performance Integrated Circuit (HPIC) Design* Laboratory

Experimentally quantified noise propagation in 3-D integrated circuits with respect to 3-D power distribution network topology

Examined various clock and power distribution schemes for 3D-IC's; MIT Lincoln Laboratory fabricated test circuits in 2007 and 2010.

Performed *RLC* modeling and characterization of 3D vias and signal integrity simulations for MIT Lincoln Laboratory's 3D-IC process.

January 2006 – June 2006: **University of Rochester Graduate Research Assistant (RA)**, *Rochester, NY*

Advised by: Profs. Martin Margala and Marc J. Feldman

Developed a 1 T-Hz ballistic deflection transistor.

Fabricated ballistic deflection transistor at Cornell University's NanoScale Science and Technology Facility (CNF).

January 2004 – May 2005: **Duke University Pratt Fellowship,** *Undergraduate Academic Researcher*

Advised by: Prof. Patrick Wolf

Enhanced Backpack Design for Brain Machine Interface. Programmed an Elf 3 ultra low power XScale PXA255 in VHDL to control the electrical frontend of the Brain Machine Interface, where the Brain Machine Interface is connected to the brain of a rhesus monkey.

May-August 2003: **University of Rochester's Laboratory for Laser Energetics,** *Undergraduate Researcher*

Advised by: Prof. Roman Sobolewski

Developed magnetic susceptibility experiment to examine transition temperatures of very small (few mm in length and width) single crystal superconducting material.

May-August 2002: **University of Rochester's Laboratory for Laser Energetics,** *Undergraduate Lab Technician*

Advised by: Prof. Roman Sobolewski

Developed functional schematic of Omega EP laser system including beamlines, mirrors, actuators, amplifiers, compression chamber, and target chamber.

June-August 2000: **University of Rochester's Laboratory for Laser Energetics,** *Academic Researcher*

Advised by: Prof. Roman Sobolewski

Selected as one of 15 (from 80 applicants) high school students to participate in the Summer Research Program. Examined Josephson Junctions using JSPICE simulations and lab experimentation.

PROFESSIONAL MEMBERSHIPS

Institute of Electrical and Electronics Engineers (IEEE) – member since 2004

Optical Society of America (OSA) – member since March 2012

American Society for Engineering Education (ASEE) – member since July 2012

National Science Teachers Association (NSTA) – member since June 2012

PROFESSIONAL SERVICE

External reviewer for

Journals

IEEE Transactions on Very Large Scale Integration (VLSI) Circuits (TVLSI); IEEE Transactions on Electron Devices (TED); IEEE Transactions on Circuits and Systems-II (TCAS-II); IEEE Transactions on Computer-Aided Design (TCAD); IEEE Transactions on Electron Device Letters (TEDL); ASP Journal of Low Power Electronics (JOLPE); Analog Integrated Circuits and Signal Processing (ALOG); Microelectronics Journal, IEEE Transactions on Advanced Packaging (TADVP); IEEE Transactions on Components, Packaging and Manufacturing Technology (TCPMT)

Conferences

Design, Automation, and Test in Europe (DATE); International Symposium on Circuits and Systems (ISCAS); International Conference on Computer Design (ICCD); System-on-Chip Conference (SoCC); Asia Pacific Conference on Circuits and Systems (APCCAS); International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS); International Symposium on Networks-on-Chip (NoCS); Great Lakes Symposium on VLSI (GLSVLSI)

Graduate Organizing Group Department Representative – University of Rochester, Spring 2010-2012.

IEEE graduate president – University of Rochester, Fall 2006- Spring 2007.

IEEE undergraduate secretary student body board member – Duke University, 2004-2005.

Duke University Alumni interview program – Interviewed over 15 potential undergraduate candidates for admittance to Duke since Spring 2007.

University of Rochester GEAR program interviewer – Interviewed 8 students for prestigious 5 year B.S/M.S. program with tuition waver – Spring 2009 and 2010.

Volunteer for the Duke Readers Project since Fall 2010 – The Duke Readers Project matches current Duke undergraduates with alumni that provide comments and suggestions on written work for designated courses.

Volunteer for the Finger Lakes FIRST (For Inspiration and Recognition of Science and Technology) LEGO League Tournament since December 2008.

Hosted guest lecturer from IBM Research, Yorktown Heights, NY on January 2007 – Dr. Barry Rubin presented a seminar and workshop on a fullwave electromagnetic toolset developed by IBM. I was his guide around the university and department, setup the projector for his presentation, reserved the appropriate rooms for the seminar and workshop, and was the intermediary for any questions about the tool prior to and after Dr. Rubin's visit.

NON-ACADEMIC SERVICE

Monroe County Democratic Committee member – petitioned representative of the Gates Democratic Committee since Fall 2009, Town of Gates, 21st Electoral District, Rochester, NY 14606.

- Campaign and fundraise for candidates (candidate petitioning, phone banks, campaign lawn signs)
- Support local elected officials
- Organize community events such as picnics, yard sales, holiday celebrations
- Monthly community cleanup of town parks and pedestrian walkways (April through November)

Greek Pontiac Society – committee member, Fall 2009 – Spring 2012.

- Organized community dances, meet and greets, and cultural education events

Licensed soccer coach for youth teams since 2010, Rochester, NY

- National D licensed soccer coach for the Empire United Soccer Academy (2011-2012), Greece Cobras Footbal Club (2011-2012), and Gates Metros (2010).
- Develop detailed training sessions, perform player evaluations, and organize tournament and game schedules.

TEACHING

Academic Experience

September 2011 – May 2012 : University of Rochester Kearn Center Tutor, *Rochester, NY*

One on one tutoring of under-represented minorities in *Calculus* (MTH 141) and *Introduction to Signals and Circuits* (ECE 111) through the Kearn Center (mission to provide education opportunities and assistance for low-income,

first-generation college, and underrepresented minority students).

September 2005 – May 2007 : University of Rochester Teaching Assistant (TA), [Rochester, NY]

Prepared, organized, and guided students through lab exercises and course material for *Logic Design* (ECE 112L, undergraduate logic design), *Circuits and Microcontrollers for Scientists and Engineers* (ECE 210L, undergraduate class), and *Performance Issues in IC/VLSI Design and Analysis* (ECE 465, graduate class). Held one-on-one office hours, group based learning sessions, laboratory assistance, and recitations.

September 2004 – May 2005 : Duke University Teaching Assistant (TA), [Durham, NC]

Prepared, organized, and guided students through *Introduction to Electronics: Integrated Circuists* (ECE 331L) laboratory exercises and recitations.

Non-Academic Experience

September 2006 – June 2011 : Tutored 7 to 11 year olds in the Greek language (my 10 year old son included)

January 2007 – February 2012 : Taught 7 to 13 year olds Greek and Pontiac dance (my 10 year old son included)

October 2010 – Present : Soccer coach for the Empire United Soccer Academy (2011-2012), Greece Cobras Footbal Club (2011-2012), and Gates Metros (2010) (my 10 year old son included).

Mentoring Experience

HPIC Electrical Engineering Program, University of Rochester, Rochester, NY, Dec. 2011 to Aug. 2012

Mentored Mr. Boris Vaisband as a new member to High Performance Integrated Circuit lab group. Guided Mr. Vaisband through grant writing exercises, manuscript preparations, presentation preparations, and addressed general questions. Mr. Vaisband is continuing my research effort on 3-D integrated circuits, and was therefore further mentored on this topic, with a particular emphaisis on power delivery in 3-D circuits.

Electrical Engineering Exchange Program, University of Rochester, Rochester, NY, Sept. 2009 to June 2010

Supervisor for Jinhui Wang, Joint Education Ph.D. student from the Beijing University of Technology. Mentored Mr. Wang through a project that explored thermal coupling induced by junction resistances of vertical cavity surface emitting lasers (VCSEL), and a project focused on power delivery in 3-D integrated circuits. Currently is an Assistant Professor at Beijing University of Technology.

HPIC Electrical Engineering Program, University of Rochester, Rochester, NY, Sept. 2009 to Oct. 2010

Mentored Mr. Ravi Patel as a new member to High Performance Integrated Circuit lab group. Guided Mr. Patel through grant writing exercises, manuscript preparations, presentation preparations, and addressed general questions.

Education and Teaching Conferences

Technical reviewer for American Society for Engineering Education (ASEE) Annual Conference

Member of Teaching Organizations

American Society for Engineering Education

National Science Teachers Association

The Chronicle of Higher Education

Additional Training

Future Faculty Initiave Workshop Series, University of Rochester, September 2011 to May 2012

Topics included: "The Faculty Role," "Learner Centered Teaching," "Assessing Learning in the Classroom," "Opportunities in Diversity: Tapping the Multiplicity of Experience," and "What is a Mentor and What Good is Having One?"

Active participant of the University Committee for Interdisciplinary Studies (UCIS) Leadership in Education Cluster, University of Rochester, September 2006 to June 2012 (renamed September 2009)

Informal gatherings of faculty, staff, graduate students, and postdoctoral fellows from different departments and colleges in the university to discuss research literature on teaching – discussion based lunchtime seminars

Activities designed to offer ideas on how students learn (metacognition, student-centered teaching, peer instruction, constructivism, motivation, discover-based learning, etc.), analysis of various teaching methods, and

provide insight on the teaching component for new faculty hires

Topics covered included, but were not limited to:

Tactics for incorporating current educational research into your teaching to facilitate an engaging and interactive class

Curriculm and assessment research – development of fair and quantifiable questions for exams and homework; proper testing of student acquired knowledge

Active and cooperative learning – peer leaders based teaching method

Faculty role and responsibilities as applied to teaching – time management, lesson planning, course development, training and mentoring techniques, various pedagogical techniques

Student misconceptions – student attitudes about courses and learning

Development of teaching skills and approaches – assessment of teaching strategies for enhancing student learning: inquiry-based learning, service learning, case discussions, problem-based learning, problem manipulation, workshop methods, and other pedagogical techniques

Employing technologies in the classroom – clickers, social networking, Blackboard, smartphones, tablets

Resources available to new faculty –

"When to help students and when to seek help" – helping students in distress

Universal Course Design – designing courses to make classroom learning accessible to all students no matter their individual backgrounds; strategies focus on four key principles: curriculum, instruction, assessment, and environment; evaluation of course material to adapt curriculum to meet student strengths

Active participant of the Center for Excellence in Teaching and Learning (CETL), University of Rochester, January 2010 to present

CETL staff provide literature and expertise on teaching methodologies, course development, student assessment, lecture preparation, course objectives, and other teaching relavent topics

Participated in CETL sponsored teaching workshops on "Assessing student learning across the semester: from objectives to exams," and "So you've been given a (new) course to teach: Now what?"

Member of the Center for Integration of Research, Teaching and Learning (CIRTL) – April 2012 to present

NSF-sponsored national center dedicated to teaching and learning

University of Rochester joined CIRTL in Spring 2012 (1 of 25 member universities)

CIRTL mission to enhance undergraduate education through the implementation and advancement of effective teaching practices:

Achieved through three CIRTL pillars of teaching as research, learning communities, and learning through diversity

Resources include Interdisciplinary cross-network learning communities, coffee hours, online conference rooms, Moodle

CIRTL offers MOOC-like (massive open online courses) teaching related course work including "The College Classroom," "Creating a Collaborative Learning Environment," "Effective Teaching with Technology," "Instructional Materials Development Course," and many others

Enrolled in "The College Classroom" MOOC, Fall 2012 – explore teaching philosophy, design course curriculum, learn to monitor and investigate the effectiveness of the learning environment, explore meaning of an inclusive classroom environment to engage all students, compare various pedagogical methods (POGIL, PLTL, PBL, etc.), emphasis on learning centered classroom

SKILLS AND HOBBIES

Computer

Computer Languages: Assembly (MIPS, Intel x86), VHDL, Verilog, C++/C, Java, SVRF scripting language, Perl, TVF, and Tcl/Tk.

Networking programs: Tera Term, WS_FTP, SSH Client.

Competency in: Sun (Unix), Apple (MacOS), and PCs (Windows/Linux).

Proficiency with: Pspice, Jspice, Hspice, Latex, Microsoft Word, Excel, Powerpoint, Maple, Adobe Illustrator, Matlab, Powerview, LabVIEW, Max + Plus II, Espresso, Mathematica, Mentor Graphics (ic & da), Cadence (Virtuoso , Assura, Analog Environment, & Encounter), CalibreDRV, Agilient ADS, Quicksim, Asitic, Comsol Multiphysics, Ansoft (Quick 3-D & HFSS).

Lab equipment

Agilent E8364A 45 MHz to 50 GHz PNA series network analyzer

HP 54750A digitizing oscilloscope

HP 4145B Semiconductor parameter analyzer

Agilent 8565E spectrum analyzer

West-Bond 7400 ultrasonic, thermosonic, and thermocompression wire bonding methods

CASCADE MicroTech probe station for 100 μm and 150 μm pitch single-ended and differential signal high-frequency probing

Interests

Chess, soccer, reading non-fiction (in addition to technical magazines – Times, Bloomberg Businessweek, Wired, Bloomberg Markets, Popular Mechanics), photography, dance, traveling, and spending time with my 10 year old son.

Languages: English (Native), Greek (fluency in speech, reading, and writing)