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RESEARCH AND TEACHING INTERESTS

- Large scale digital, analog, and mixed-signal integrated circuits, containing RF transmitters, sensors, analog-to-digital converters, and high speed digital cores.
- Modeling and analysis of complex structures such as on-chip interconnects, power/clock distribution networks, and the monolithic substrate that support these various circuits.
- Circuit level design considerations for emerging technologies such as nanowire and graphene are of particular interest, focusing on systems level integration with traditional CMOS technology.
- Systems integration of disparate technology such as III-V semiconductors, RF, and optics, with 3-D integration or silicon carrier based techniques providing the means to merge these heterogeneous technologies
- 3-D integrated circuits with an emphasis on electrical and thermal modeling and characterization, signal and power integrity, and power and clock delivery for 3-D stacking technologies.
- Interconnect related issues in 2-D and 3-D integrated circuits
- Power management for SoC and microprocessor circuits
- Security-aware integrated circuit design including logic encryption/obfuscation, attack detection and recovery, and algorithms and methodologies for design automation
- Ultra low-power sub/near-threshold circuit techniques and methodologies
- Implement pedagogical techniques, including effective evidence-based teaching practices, that incorporate learner centered teaching, technology in the classroom (clickers, web based media, etc.), and assessment based learning. Courses of interest include digital VLSI circuit design, mixed signal/analog design, digital logic, and device physics (MOS, BJT, and emerging technologies such as graphene and nanowires)

EDUCATION

University of Rochester, Rochester, NY; *Ph.D. Electrical and Computer Engineering*, advised by Prof. Eby G. Friedman., Dissertation entitled *Characterization and Modeling of TSV Based 3-D Integrated Circuits,* graduation August 2013.

University of Rochester, Rochester, NY; *M.S. Electrical and Computer Engineering*, May 2007.
Cumulative GPA: 3.85/4.0

Relevant course work: Semiconductor Devices; Digital Integrated Circuit Design; RF Integrated Circuits; Performance Issues in VLSI/IC; Advanced Analog CMOS Integrated Circuit Design II; Random Processes

Duke University, Durham, NC; *B.S.E. Electrical and Computer Engineering; Biomedical Engineering*, May 2005.
Cumulative GPA: 3.18/4.0; Engineering GPA: 3.44/4.0

Relevant course work: Semiconductor Electronic Devices; Linear Systems; Switch Theory; Computer Architecture; Integrated Circuits; Electromagnetics; Advanced Semiconductor Devices; Full Custom VLSI design; IC design; Program Design/Analysis II, Bioelectricity, Fundamentals of Biomaterials and Biomechanics, Intro to Biomaterials,

Biomedical Electronics

Continuing education: Enrolled in Massive Online Open Courses (MOOC) through Coursera, edX, Udacity, and CIRTL

Completed *VLSI CAD: Logic to Layout* (Prof. Rob Rutenbar, Unversity of Illinois at Urbana-Champaign), *The College Classroom* (Profs. Peter Newbury and Elizabeth Simon, University of California, San Diego), *Teaching-as-Research in STEM Courses* (Prof. Bethany Stone)

RESEARCH – AWARDS/PUBLICATIONS/GRANTS

Awards/Recognition

Senior Member - IEEE, October 2018.

NSF CAREER for "Parameter Obfuscation: A Novel Methodology for the Protection of Analog Intellectual Property," April 2018.

2018 IEEE Philadelphia Section Delaware Valley Young Electrical Engineer of the Year Award for contributions in hardware security and trust. Specifically, for the obfuscation of digital and analog circuits through novel algorithms and methodologies that secure intellectual property from reverse engineering, cloning, and counterfeiting.

IEEE International Symposium on Circuits and Systems (ISCAS '08) Best Paper Award Finalist; paper [61] was selected as one of ten papers for a special poster session competing for the Best Paper Award.

University of Rochester Dean's Fellowship, two-year, merit based fellowship, University of Rochester, Sept. 2005 – May 2007.

IEEE Southeast Regional Top 10 Paper Finalist; paper [62] was selected as one of ten papers that was then presented at IEEE SoutheastCon 2004.

Duke University Pratt Fellows Program; one and a half year engineering fellowship, Duke University, January 2004 – May 2005.

Publications

Total Citation Count of 1572; h-index of 17 (Google scholar)

Book

[1] V. Pavlidis, I. Savidis, and E. G. Friedman, Three-Dimensional Integrated Circuit Design, 2nd Edition, Morgan Kaufmann Publishers, Elsevier, pp. 1-768, 2017, ISBN # 978-0-12-410484-6.

Book Chapters

[1] I. Savidis and E. G. Friedman, "Physical Design Trends for Interconnects," *On-Chip Communication Architectures System on Chip Interconnect*, S. Pasricha and N. Dutt, Morgan Kaufmann Publishers, Elsevier, Chapter 11, pp. 403-437, 2008, ISBN # 978-0-12-373892-9.

Dissertation

[1] I. Savidis, *Characterization and Modeling of TSV Based 3-D Integrated Circuits*, Ph.D. Dissertation, University of Rochester, August 2013.

Journal Papers

[1] K. Juretus and I. Savidis, "Synthesis of Hidden State Transitions for Sequential Logic Locking," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 40, No. 1, pp. 11 – 23, January 2021.

[2] K. Juretus and I. Savidis, "Inreased Output Corruption and Structural Attack Resiliency for SAT Attack Secure Logic Locking," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 40, No. 1, pp. 38 – 51, January 2021.

[3] M. Jacovic, K. Juretus, N. Kandasamy, I. Savidis, and K. Dandekar, "Physical Layer Encryption for Wireless OFDM Communication Systems," *Journal of Hardware and Systems Security (HaSS)*, Vol. 4, No. 3, pp. 230-245, September 2020.

[4] M. S. Hossain and I. Savidis, "Dynamic Differential Signaling Based Logic Families for Robust Ultra-low

Power Near-threshold Computing," *Microelectronics Journal*, Vol. 102, No. 9, pp. 1-14, May 2020 (online).

[5] M. S. Hossain and I. Savidis, "Recycling of Unused Leakage Current for Energy Efficient Multi-Voltage," *Microelectronics Journal*, Vol. 101, No. 7, pp. 1-16, April 2020 (online).

[6] K. Juretus and I. Savidis, "Characterization of In-Cone Logic Locking Resiliency Against the SAT Attack," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 39, No. 8, pp. 1607-1620, August 2020.

[7] J. Chacko, K. Juretus, M. Jacovic, C. Sahin, N. Kandasamy, I. Savidis, and K. Dandekar, "Securing Wireless Communication via Hardware-Based Packet Obfuscation," *Journal of Hardware and Systems Security*, pp. 1-12, May 2019.

[8] D. Pathak and I. Savidis, "On-Chip Power Supply Noise Suppression Through Hyperabrupt Junction Varactors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 26, No. 11, pp. 2230-2240, November 2018.

[9] M. K. Tavana, M. H. Hajkazemi, D. Pathak, I. Savidis, and H. Homayoun, "ElasticCore: A Dynamic Heterogeneous Platform with Joint Core and Voltage/Frequency Scaling," *IEEE Transactions on Very Large Scale Integration*, Vol. 26, No. 2, pp. 249-261, February 2018.

[10] D. Pathak, H. Homayoun, and I. Savidis, "Smart Grid on Chip: Work Load-Balanced On-Chip Power Delivery," *IEEE Transactions on Very Large Scale Integration*, Vol. 25, No. 9, pp. 2538-2551, September 2017.

[11] I. Savidis, B. Ciftcioglu, J. Xu, J. Hu, M. Jain, R. Berman, J. Xue, P. Liu, D. Moore, G. Wicks, M. Huang, H. Wu, E. G. Friedman, "Heterogeneous 3-D Circuits: Integrating Free-Space Optics with CMOS," *Microelectronics Journal*, Vol. 50, No. 4, pp. 66-75, April 2016.

[12] I. Savidis, B. Vaisband, and E. G. Friedman, "Experimental Analysis of Thermal Coupling in 3-D Integrated Circuits," *IEEE Transactions on Very Large Scale Integration*, Vol. 23, No. 10, pp. 2077-2089, October 2015.

[13] I. Savidis, S. Kose, and E. G. Friedman, "Power Noise in TSV-Based 3-D Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 48, No. 2, pp. 587-597, February 2013.

[14] B. Ciftcioglu, R. Berman, S. Wang, J. Hu, I. Savidis, M. Jain, D. Moore, M. Huang, E. G. Friedman, G. Wicks, and H. Wu, "3-D Integrated Heterogeneous Intra-Chip Free-Space Optical Interconnect," *Optics Express*, Vol. 20, No. 4, pp. 4331-4345, February 2012.

[15] V. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks in 3-D Integrated Systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 12, pp. 2256-2266, December 2011.

[16] J. Wang, I. Savidis, and E. G. Friedman, "Thermal Analysis of Oxide-Confined VCSEL Arrays," *Microelectronics Journal*, Vol. 42, No. 5, pp. 820-825, May 2011.

[17] B. Ciftcioglu, R. Berman, J. Zhang, Z. Darling, S. Wang, J. Hu, J. Xue, A. Garg, M. Jain, I. Savidis, D. Moore, M. Huang, E. G. Friedman, G. Wicks, and H. Wu, "A 3-D Integrated Intra-Chip Free-Space Optical Interconnect for Many-Core Chips," *IEEE Photonics Technology Letters*, Vol. 23, No. 3, pp. 164-166, February 2011.

[18] I. Savidis, S. M. Alam, A. Jain, S. Pozder, R. E. Jones, and R. Chatterjee, "Electrical Modeling and Characterization of Through-Silicon vias (TSVs) for 3-D Integrated Circuits," *Microelectronics Journal*, Vol. 41, No. 1, pp. 9-16, January 2010.

[19] I. Savidis and E. G. Friedman, "Closed-Form Expressions of 3-D Via Resistance, Inductance, and Capacitance," *IEEE Transactions on Electron Devices*, Vol. 56, No. 9, pp. 1873-1881, September 2009.

Conference Papers

[1] Z. Wu and I. Savidis, "Variation-aware Analog Circuit Sizing with Classifier Chains," *Proceedings of the ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, pp. 1 – 6, September 2021.

[2] M. S. Hossain and I. Savidis, "Energy Efficient Computing with Heterogeneous DNN Accelerators," *Proceedings of the IEEE International Conference on Artificial Circuits and Systems (AICAS)*, pp. 1 – 4, June 2021.

[3] S. Phatharodom, A. Sasan, and I. Savidis, "SAT-attack Resilience Measure for Access Restricted Circuits," *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 213 – 220, June 2021.

[4] S. A. Beheshti, A. Vakil, S. Manoj, I. Savidis, H. Homayoun, and A. Sasan, "A Reinforced Learning Solution for Clock Skew Engineering to Reduce Peak Current and IR Drop," *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 181 – 187, June 2021.

[5] Z. Wu and I. Savidis, "CALT: Classification with Adaptive Labeling Thresholds for Analog Circuit Sizing," *Proceedings of the ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, pp. 49 – 54, November 2020.

[6] V. V. Rao, K. Juretus, and I. Savidis, "Security Vulnerabilities of Obfuscated Analog Circuits," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1 – 5, October 2020.

[7] K. Juretus and I. Savidis, "Reducing Logic Locking Key Leakage Through the Scan Chain," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1 – 5, October 2020.

[8] S. Phatharodom, N. Kandasamy, and I. Savidis, "Modeling SAT-attack Search Complexity," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1 – 5, October 2020.

[9] M. S. Hossain and I. Savidis, "Dynamic Idle Core Management and Leakage Current Reuse in MPSoC Platforms," *Proceedings of the ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 49 – 54, August 2020.

[10] S. Phatharodom, N. Kandasamy, and I. Savidis, "Closed-form Estimation of SAT-attack Resilience," *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, pp. 1 – 6, March 2020.

[11] V. V. Rao and I. Savidis, "Multi-objective Simulation-based Optimization of Analog Tranistor Sizing," *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, pp. 1 – 6, March 2020.

[12] D. Pathak and I. Savidis, "Applying Swarm Intelligence to Distributed On-chip Power Management," *IEEE Proceedings of the International Conference on Computer Design (ICCD)*, pp. 532-540, November 2019.

[13] D. Pathak and I. Savidis, "Evolving On-chip Power Delivery Through Particle Swarm Optimization," *IEEE/ACM Proceedings of the Workshop on Machine Learning for CAD (MLCAD)*, pp. 1-6, September 2019.

[14] R. Kuttappa, B. Taskin, S. Lerner, V. Pano, and I. Savidis, "Robust Low Power Clock Synchronization for Multi-Die Systems," *Proceedings of the IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 1 – 6, July 2019.

[15] V. V. Rao and I. Savidis, "Mesh Based Obfuscation of Analog Circuit Properties," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1-5, May 2019.

[16] K. Juretus and I. Savidis, "Increasing the SAT Attack Resiliency of In-Cone Logic Locking," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1-5, May 2019.

[17] M. S. Hossain and I. Savidis, "Resusing Leakage Current for Improved Energy Efficiency of Multi-Voltage Systems," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1-5, May 2019.

[18] K. Juretus, V. V. Rao, and I. Savidis, "Securing Analog Mixed-Signal Integrated Circuits Through Shared Dependencies," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 483-488, May 2019.

[19] M. S. Hossain and I. Savidis, "Multi-Voltage Domain Power Distribution Network for Optimized Ultra-low Voltage Clock Delivery," *Proceedings of the IEEE International Green and Sustainable Computing Conference (IGSC)*, pp. 244-251, October 2018.

[20] V. V. Rao and I. Savidis, "Transistor Sizing for Parameter Obfuscation of Analog Circuits Using Satisfiability Module Theory," *Proceedings of the IEEE International Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 102-106, October 2018.

[21] K. Juretus and I. Savidis, "Importance of Multi-parameter SAT Attack Exploration for Integrated Circuit Security," *Proceedings of the IEEE International Asia Pacific Conference on Circuits and Systems (APCCAS)*, pp. 366-369, October 2018.

[22] D. Werner, K. Juretus, I. Savidis, and M. Hempstead, "Machine Learning on the Thermal Side-Channel: Analysis of Accelerator-rich Architectures," *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 83-91, October 2018.

[23] F. Castro, I. Savidis, and A. Sarmiento, "A Quasi-analytic Behavioral Model for the Single-electron Transistor

for Hybrid MOS/SET Circuit Simulation," *Proceedings of the IEEE Nanotechnology Materials and Devices Conference (NMDC)*, pp. 1-4, October 2018.

[24] K. Juretus and I. Savidis, "Time Domain Sequential Locking for Increased Security," *Proceedings of the International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, May 2018.

[25] M. S. Hossain and I. Savidis, "Noise Constrained Optimum Selection of Supply Voltage for IoT Applications," *Proceedings of the International Symposium on Circuits and Systems (ISCAS)*, pp. 1-5, May 2018.

[26] K. Juretus and I. Savidis, "Enhanced Circuit Security Through Hidden State Transitions," *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, pp. 781-784, March 2018.

[27] V. V. Rao and I. Savidis, "Security Oriented Analog Circuit Design Using Satisfiability Modulo Theory Based Search Space Exploration," *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, pp. 770-774, March 2018.

[28] H. Sayadi, D. Pathak, I. Savidis, and H. Homayoun, "Power Conversion Efficiency-aware Mapping of Multithreaded Applications on Heterogeneous Architectures: A Comprehensive Parameter Tuning," *Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 70-75, January 2018.

[29] M. S. Hossein and I. Savidis, "Bi-directional Input/Output Circuits with Integrated Level Shifters for Near-Threshold Computing," *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1240-1243, August 2017.

[30] I. Daulagala and I. Savidis, "Clock Tree Synthesis for Heterogeneous 3-D Integrated Circuits," *Proceedings of the ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP),* pp. 1-6, May 2017.

[31] D. Pathak, H. Homayoun, and I. Savidis, "Work Load Scheduling for Multi-Core Systems with Under-Provisioned Power Delivery," *Proceedings of the ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 387-392, May 2017.

[32] V. V. Rao and I. Savidis, "Protecting Analog Circuits with Parameter Biasing Obfuscation," *Proceedings of the IEEE Latin American Test Symposium (LATS)*, pp. 1-6, March 2017.

[33] J. Chacko, K. Juretus, M. Jacovic, C. Sahin, N. Kandasamy, I. Savidis, and K. R. Dandekar, "Physical Gate Based Preable Obfuscation for Securing Wireless Communication," *IEEE International Conference on Computing, Networking and Communication (ICNC)*, (accepted), January 2017.

[34] K. Siozios, I. Savidis, and D. Soudris, "A Framework for Exploring Alternative Fault-Tolerant Schemes Targeting 3-D Reconfigurable Architectures," *Proceedings of the IEEE Workshop on Virtual Prototyping of Parallel and Embedded Systems (ViPES)*, pp. 1 – 6, July 2016.

[35] K. Juretus and I. Savidis, "Reducing Logic Encryption Overhead Through Gate Level Key Insertion," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS),* pp. 1714-1717, May 2016.

[36] M. S. Hossain and I. Savidis, "Robust Near-threshold Inverter with Improved Performance for Ultra-Low Power Applications," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS),* pp. 738-741, May 2016.

[37] D. Pathak, M. H. Hajkazemi, M. K. Tavana, H. Homayoun, and I. Savidis, "Energy Efficient On-Chip Power Delivery with Run-Time Voltage Regulator Clustering," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS),* pp. 1210-1213, May 2016.

[38] K. Juretus and I. Savidis, "Reduced Overhead Gate Level Logic Encryption," *Proceedings of the IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 15-20, May 2016.

[39] D. Pathak, M. H. Hajkazemi, M. K. Tavana, H. Homayoun, and I. Savidis, "Load Balanced On-Chip Power Delivery for Average Current Demand," *Proceedings of the IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI)*, pp. 439-444, May 2016.

[40] K. Juretus and I. Savidis, "Low Overhead Gate Level Logic Encryption," *Government Microcircuit Applications & Critical Technology Conference*, pp. 455-459, March 2016.

[41] M. S. Hossain and I. Savidis, "Dynamic Current Mode Inverter for Ultra-Low Power Near-Threshold Computing," *Government Microcircuit Applications & Critical Technology Conference*, pp. 409-412, March 2016.

[42] K. Juretus and I. Savidis, “Securing Integrated Circuits Through Gate-Level Logic Encryption,” *2015 Defense Innovation Summit*, pp. 1, December 2015.

[43] M. K. Tavana, D. Pathak, M. H. Hajkazemi, I. Savidis, H. Homayoun, “Realizing Complexity-Effective On-Chip Power Delivery for Many-Core Platforms by Exploiting Optimized Mapping,” *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, pp. 581-588, October 2015.

[44] M. K. Tavana, M. H. Hajkazemi, D. Pathak, I. Savidis, and H. Homayoun, “ElasticCore: Enabling Dynamic Heterogeneity with Joint Core and Voltage/Frequency Scaling,” *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 1-6, June 2015.

[45] D. Pathak and I. Savidis, “Power Supply Voltage Detection and Clamping Circuit for 3-D Integrated Circuits,” *Proceedings of the IEEE International SOI-3D-Subthreshold Microelectronics Technology Unified Conference*, pp. 1-3, October 2014.

[46] D. Pathak and I. Savidis, “Run-Time Voltage Detection Circuit for 3-D IC Power Delivery,” *Proceedings of the IEEE International System-on-Chip (SoC) Conference*, pp. 183-187, September 2014.

[47] B. Vaisband, I. Savidis, and E. G. Friedman, “Thermal Conduction Path Analysis in 3-D ICs,” *Proceedings of the IEEE Symposium on Circuits and Systems*, pp. 594-597, June 2014.

[48] I. Savidis and E. G. Friedman, “Thermal Coupling in TSV-Based 3-D Integrated Circuits,” *Proceedings of the Workshop on 3-D Integration, Design, Automation & Test in Europe Conference*, March 2014.

[49] I. Savidis and E. G. Friedman, “Test Circuits for 3-D Systems Integration,” *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, pp. 181-184, March 2012.

[50] H. Wu, B. Ciftcioglu, R. Berman, S. Wang, J. Hu, I. Savidis, M. Jain, D. Moore, M. Huang, E. Friedman, and G. Wicks, “Chip-Scale Demonstration of 3-D Integrated Intra-Chip Free-Space Optical Interconnect (Invited Paper),” *Photonics West: Proceedings of SPIE Optoelectronic Integrated Circuits XIV,* Vol. 8265, pp. 82650C-1 – 82650C-10, February 2012.

[51] I. Savidis, V. Pavlidis, and E. G. Friedman, “Clock Distribution Models of 3-D Integrated Systems,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2225-2228 May 2011.

[52] I. Savidis, S. Kose, and E. G. Friedman, “Power Grid Noise in TSV-Based 3-D Integrated Systems,” *Proceedings of the Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, pp. 129-132, March 2011.

[53] B. Ciftcioglu, R. Berman, J. Zhang, Z. Darling, A. Garg, J. Hu, M. Jain, P. Liu, I. Savidis, S. Wang, J. Xue, E. G Friedman, M. Huang, D. Moore, G. Wicks, and H. Wu, “Initial Results of Prototyping a 3-D Integrated Intra-Chip Free-Space Optical Interconnect,” *Proceedings of the Workshop on the Interaction between Nanophotonic Devices and Systems (WINDS 2010)*, December 2010.

[54] J. Xue, A. Garg, B. Ciftcioglu, J. Hu, S. Wang, I. Savidis, M. Jain, R. Berman, P. Liu, M. Huang, H. Wu, E. Friedman, G. Wicks, and D. Moore, "An Intra-Chip Free-Space Optical Interconnect," *ISCA '10: Proceedings of the 37th Annual International Symposium on Computer Architecture*, pp. 94-105, June 2010.

[55] B. Ciftcioglu, R. Berman, J. Zhang, Z. Darling, S. Wang, J. Hu, J. Xue, A. Garg, M. Jain, I. Savidis, D. Moore, M. Huang, E. G. Friedman, G. Wicks, and H. Wu, “3-D Integrated Intra-Chip Free-Space Optical Interconnect,” *2010 IEEE International Solid-State Circuits Conference (ISSCC) Student Research Forum*, February 2010.

[56] J. Xue, A. Garg, B. Ciftcioglu, S. Wang, I. Savidis, J. Hu, M. Jain, M. Huang, H. Wu, E. G. Friedman, G. W. Wicks, and D. Moore, "An Intra-Chip Free-Space Optical Interconnect," *Proceedings of the 3rd Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI '09) held in conjunction with the 36th International Symposium on Computer Architecture*, June 2009.

[57] I. Savidis, E. G. Friedman, V. F. Pavlidis, and G. De Micheli, "Clock and Power Distribution Networks for 3-D Integrated Circuits," *Proceedings of the Workshop on 3D Integration, Design, Automation & Test in Europe Conference,* March 2009.

[58] I. Savidis, S. M. Alam, A. Jain, S. Pozder, R. E. Jones, and R. Chatterjee, “Electrical Modeling and Characterization of Through-Silicon vias (TSVs) for 3-D Integrated Circuits,” *Proceedings of VLSI/ULSI Multilevel Interconnect Conference (VMIC)*, pp. 181-186, Oct. 2008.

[59] V. F. Pavlidis, I. Savidis, and E. G. Friedman, “Clock Distribution Architectures for 3-D SOI Integrated

Circuits," *Proceedings of the IEEE International SOI Conference,* pp. 111-112, October 2008.

[60] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks for 3-D Integrated Circuits," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 651-654, September 2008.

[61] I. Savidis and E. G. Friedman, "Electrical Modeling and Characterization of 3-D Vias," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 784-787, May 2008.

[62] I. Savidis, A. Jukna, and R. Sobolewski, "Contactless Determination of T_c in Very Small Single Crystal MgB_2 and Thin Film YBCO," *IEEE Student Paper Contest SoutheastCon 2004*, March 2004.

[63] I. Savidis, and R. Sobolewski, "Characterization of Josephson Junctions," *University of Rochester Journal*, August 2000.

Patents

[1] M. S. Hossain and I. Savidis, "Energy Efficiency of Heterogeneous Multi-voltage Domain Deep Neural Network Accelerators Through Leakage Reuse for Near-memory Computing Applications," U.S. Patent, 63/196,709, June 4, 2021.

[2] M. S. Hossain and I. Savidis, "Charge Recycling from Idle Circuits for Improved Energy Efficiency of Multi-voltage Systems," U.S. Patent, 17/307,118, May 4, 2021.

[3] D. Pathak and I. Savidis, "On-chip Voltage Assignment Through Particle Swarm Optimization," U.S. Patent, 17/271,121, February 24, 2021.

[4] K. J. Juretus and I. Savidis, "Enhanced Circuit Security Through Hidden State Transitions," Patent Pending, 16/980,471, Filed September 14, 2020.

[5] I. Savidis, V. V. Rao, and K. J. Juretus, "Securing Analog Mixed-Signal Integrated Circuits Through Shared Dependencies," U.S. Patent, 16/862,111, Filed April 29, 2020.

[6] V. V. Rao and I. Savidis, "Transistor Sizing for Parameter Obfuscation of Analog Circuits," U.S. Patent, 16/778,550, Filed January 31, 2020.

[7] J. J. Chacko, K. R. Dandekar, M. Jacovic, K. J. Juretus, N. Kandasamy, C. Sahin, I. Savidis, "Physical Gate Based Preamble Obfuscation for Securing Wireless Communication," U.S. Patent, 16/478,148, July 16, 2019.

[8] D. Pathak and I. Savidis, "On-chip Power Supply Noise Suppression Through Hyperabrupt Junction Varactors," U.S. Patent, 16/448,019, File June 21, 20219.

[9] K. R. Dandekar, J. J. Chacko, K. J. Juretus, M. Jacovic, C. Sahin, N. Kandasamy, and I. Savidis, "Physical Layer Key based Interleaving for Secure Wireless Communication," U.S. Patent, 16/432,509, June 5, 2019.

[10] K. J. Juretus and I. Savidis, "Increasing the Resliency of In-Cone Logic Locking Against the SAT Attack Through Maximum Fanout Free Cones," Provisional Patent, 62/798,282, Filed January 29, 2019.

[11] D. Pathak and I. Savidis, "An Under-Provisioned Reconfigurable On-chip Power Delivery Network," Patent Pending, 62/492,681, May 1, 2018.

[12] K. Juretus and I. Savidis, "Enhanced Circuit Security Through Hidden State Transitions," Provisional Patent, 62/642,128, Filed March 13, 2018.

[13] J. J. Chacko, K. J. Juretus, M. Jacovic, C. Sahin, N. Kandasamy, I. Savidis, and K. R. Dandekar, "Physical Layer Key Based Pilot Encryption for Secure Wireless Communication," Provisional Patent, DPX.P047.US.60, Filed June 9, 2017.

[14] D. Pathak and I. Savidis, "Work Load Scheduling for Multi Core Systems with Under-Provisioned Power Delivery," Provisional Patent, DPX.P044.US.60, Filed May 1, 2017.

[15] V. V. Rao, K. J. Juretus, and I. Savidis, "Protecting Analog Circuits with Parameter Biasing Obfuscation," Provisional Patent, DPX.P043.US.60, Filed March 10, 2017.

[16] K. Juretus and I. Savidis, "Reduced Overhead Gate Level Logic Encryption," Patent Pending, DRX.P020.WO.01, Filed October 24, 2016.

[17] D. Pathak and I. Savidis, "Power Supply Voltage Detection and Power Delivery Circuit," U.S. Patent 15/096,046, Issued October 13, 2016.

[18] K. Juretus and I. Savidis, "Low Overhead Gate Level Logic Encryption," Provisional Patent, DRX.P020.US.60, Filed October 23, 2015.

[19] D. Pathak and I. Savidis, "Run-Time Power Supply Voltage Detection and Clamping Circuit," Provisional Patent, DRX.P009.US.60, Filed April 10, 2015.

Workshop Presentations

[1] I. Savidis, "Securing Analog/RF Intellectual Property: Split Manufacturing, Multi-Vt Devices, and Beyond," *IEEE Radio Frequency Integrated Circuits Symposium Workshop*, Boston, MassachusettsJune 2019.

[2] I. Savidis, "Research Overview – Obfuscastion of Analog Circuit Parameters," *Department of Energy – Kansas City National Security Campus*, Kansas City, Missouri, June 2019.

[3] I. Savidis, "Research Overview – Hardware Security Techniques for Analog Circuits," *Department of Energy – Kansas City National Security Campus*, Kansas City, Missouri, February 2019.

[4] I. Savidis, "Research Overview – Digital Logic Protection," *Department of Energy – Kansas City National Security Campus*, Kansas City, Missouri, February 2019.

[5] I. Savidis, "Security Oriented Analog Circuit Design Using Satisfiability Module Theory Based Search Space Exploration," *TxACE Center Texas Analog Center of Excellence STARS Workshop*, Dallas, Texas, May 2018.

[6] I. Savidis, "IP Protection Through Security-Aware Integrated Circuit Design," *Defense Advanced Research Projects Agency (DARPA) IP Theft Workshop*, Arlington, Virginia, February 2016.

[7] I. Vaisband, S. Kose, I. Savidis, and E. G. Friedman, "On-Chip Power Delivery," *CEIS University Technology Showcase*, Rochester, New York, April 6, 2011.

[8] B. Ciftcioglu, R. Berman, J. Zhang, Z. Darling, S. Wang, J. Hu, J. Xue, A. Garg, M. Jain, I. Savidis, D. Moore, M. Huang, E. G Friedman, G. Wicks, and H. Wu, "3-D Integrated Intra-Chip Free-Space Optical Interconnect", 2010 *IEEE International Solid-State Circuits Conference (ISSCC) Student Research Forum*, San Francisco, California, February 2010.

[9] I. Savidis and E. G. Friedman, "Clock Distribution Topologies for 3-D Integrated Circuits," *CEIS University Technology Showcase*, Rochester, New York, February 12, 2009.

[10] V. F. Pavlidis, I. Savidis, and E. G. Friedman, "Clock Distribution Networks for 3-D Integrated Circuits," *Massachusetts Institute of Technology Lincoln Laboratory's 3-D Integrated Circuit Multi-Project Wafer Review*, Boston, Massachusetts, September 15, 2008.

Conference Presenter

[1] Presented, "Applying Swarm Intelligence to Distributed On-chip Power Management," at the *IEEE International Conference on Computer Design*, November 2019, Abu Dhabi, United Arab Emirates.

[2] Presented, "Evolving On-Chip Power Delivery through Particle Swarm Optimization," at the *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, September 2019, Canmore, Alberta, Canada.

[3] Presented, "Transistor Sizing for Parameter Obfuscation of Analog Circuits Using Satisfiability Modulo Theory," presentation, at the *IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS)*, October 2018, Chengdu, China.

[4] Presented, "Importance of Multi-Parameter SAT Attack Exploration for Integrated Circuit Security," presentation, at the *IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS)*, October 2018, Chengdu, China.

[5] Presented, "Noise Constrained Optimum Selection of Supply Voltage for IoT Applications," at the *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, Florence, Italy.

[6] Presneted, "SMART GRID On-Chip: Load Balanced On-Chip Power Delivery," at the *IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence, Italy, May 2018.

[7] Presented, "Time Domain Sequential Locking for Increased Security," at the *IEEE International Symposium on Circuits and Systems*, Florence, Italy, May 2018.

[8] Presented, "Clock Tree Synthesis for Heterogeneous 3-D ICs," at the *ACM/IEEE System Level Interconnect Prediction Workshop (SLIP, co-located with DAC)*, San Francisco, California, June 2017.

[9] Presented, "Experimental Analysis of Thermal Coupling in TSV-Based 3-D Integrated Circuits," at the I*EEE International Symposium on Circuits and Systems (ISCAS)*, Montreal, Canada, May 2016.

[10] Presented, "Reducing Logic Encryption Overhead Through Gate Level Key Insertion," at the *IEEE International Symposium on Circuits and Systems (ISCAS),* Montreal, Canada, May 2016.

[11] Presented, "Robust Near-threshold Inverter with Improved Performance for Ultra-Low Power Applications," at the *IEEE International Symposium on Circuits and Systems (ISCAS),* Montreal, Canada, May 2016.

[12] Presented, "Energy Efficient On-Chip Power Delivery with Run-Time Voltage Regulator Clustering," at the *IEEE International Symposium on Circuits and Systems (ISCAS),* Montreal, Canada, May 2016.

[13] Presented, "Reduced Overhead Gate Level Logic Encryption," at the *IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Boston, Massachusetts, May 2016.

[14] Presented, "Load Balanced On-Chip Power Delivery for Average Current Demand," at the *IEEE/ACM Great Lakes Symposium on VLSI (GLSVLSI)*, Boston, Massachusetts, May 2016.

[15] Presented, "Low Overhead Gate Level Logic Encryption," at the *Government Microcircuit Applications & Critical Technology Conference*, Orlando, Florida, March 2016.

[16] Presented, "Dynamic Current Mode Inverter for Ultra-Low Power Near-Threshold Computing," at the *Government Microcircuit Applications & Critical Technology Conference*, Orlando, Florida, March 2016.

[17] Presented "Securing Integrated Circuits Through Gate-Level Logic Encryption," at the *2015 Defense Innovation Summit*, Austin, Texas, December 2015.

[18] Presented "Realizing Complexity-Effective On-Chip Power Delivery for Many-Core Platforms by Exploiting Optimized Mapping," at the *IEEE International Conference on Computer Design (ICCD)*, New York City, New York, October 2015.

[19] Presented "Power Supply Voltage Detection and Clamping Circuit for 3-D Integrated Circuits," at the *IEEE International SOI-3D-Subthreshold Microelectronics Technology Unified Conference*, San Francisco, California, October 2014.

[20] Presented "Run-Time Voltage Detection Circuit for 3-D IC Power Delivery," at the *IEEE International System-on-Chip (SoC) Conference*, Las Vegas, Nevada, September 2014.

[21] Presented "Thermal Coupling in TSV-Based 3-D Integrated Circuits," at the *Workshop on 3-D Integration, Design, Automation & Test in Europe Conference*, Dresden, Germany, March 2014.

[22] Presented "Test Circuits for 3-D Systems Integration," at the *Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, Orlando, Florida, March 2012.

[23] Presented "Clock Distribution Models of 3-D Integrated Systems," at the *IEEE International Symposium on Circuits and Systems (ISCAS)*, Rio de Janeiro, May 2011.

[24] Presented "Power Grid Noise in TSV-Based 3-D Integrated Systems," at the *Government Microcircuit Applications & Critical Technology Conference (GOMACTech)*, Orlando, Florida, March 2011.

[25] Presented "Clock Distribution Architectures for 3-D SOI Integrated Circuits," at the *IEEE International SOI Conference,* pp. 111-112, New Paltz, New York, October 2008.

[26] Presented "Electrical Modeling and Characterization of 3-D Vias," at the *IEEE International Symposium on Circuits and Systems (ISCAS)*, Seattle, Washington, May 2008.

[27] Presented "Contactless Determination of T_c in Very Small Single Crystal MgB_2 and Thin Film YBCO," at the *IEEE Student Paper Contest SoutheastCon 2004*, Fort Lauderdale, Florida, March 2004.

University Presentations

[1] Presented "Secure Mixed-Signal Integrated Circuits: Protection Through Obfuscation," Villanova University, November 2019.

[2] Presented "Securing Integrated Circuits Through Gate-Level Logic Encryption," Aristotle University of Thessaloniki, September 2015.

[3] Presented "Securing Integrated Circuits Through Gate-Level Logic Encryption," National Technical University of Athens (Polytechnio), August 2015.

[4] Presented "Characterization and Modeling of TSV Based 3-D Integrated Circuits," National Technical University of Athens (Polytechnio), March 2014.

[5] Presented "Characterization and Modeling of TSV Based 3-D Integrated Circuits," Northwestern University, April 2013.

[6] Presented "TSV Based 3-D Integrated Circuits," University of Illinois at Chicago, April 2013.

[7] Presented "TSV Based 3-D Integrated Circuits," Drexel University, April 2013.

[8] Presented "Characterization and Modeling of TSV Based 3-D Integrated Circuits," Rochester Institute of Technology, March 2013.

Technical Industrial/Government Presentations

[1] Cadence, "Research Overview: Hardware Security Techniques for Analog Circuits," Drexel University, Philadelphia, Pennslyvania, August 2021 (online).

[2] Cadence, "Research Overview: Hidden State Transition-based Sequential Logic Locking," Drexel University, Philadelphia, Pennslyvania, August 2021 (online).

[3] Cadence, "Research Overview: Machine Learning for Digital IC Design Automation," Drexel University, Philadelphia, Pennslyvania, July 2021 (online).

[4] Cadence, "Research Overview: Variation-aware Analog Circuit Sizing Based on Machine Learning," Drexel University, Philadelphia, Pennslyvania, July 2021 (online).

[5] DoD Software Defined Radio Working Group, "ICE Laboratory Research Overview on Hardware Security," Drexel University, Philadelphia, Pennslyvania, May 2021 (online).

[6] Lockheed Martin, "Overview of Research Activities in 3-D Integration," Drexel University, Philadelphia, Pennslyvania, June 2021.

[7] Lockheed Martin, "Research Overview: Classification with Adaptive Labeling Thresholds (CALT) for Analog Circuit Sizing," Drexel University, Philadelphia, Pennslyvania, May 2021.

[8] Lockheed Martin, "Research Overview: Energy Efficient Computing and Power Management for Ultra-low Voltage Circuits," Drexel University, Philadelphia, Pennslyvania, May 2021.

[9] Lockheed Martin, "Research Overview: Analog HW Security and EDA," Drexel University, Philadelphia, Pennslyvania, May 2021.

[10] Lockheed Martin, "Research Overview: Digital Security and ML/AI Algorithms for Electronic Design Automation," Drexel University, Philadelphia, Pennslyvania, May 2021.

[11] Lockheed Martin, "Research Overview: Field Programmable Analog Array and Analog to Digital Conversion," Drexel University, Philadelphia, Pennslyvania, May 2021.

[12] Air Force Research Laboratory – Wright Patterson Air Force Base, "Progress Update – Temporal Circuit Obfuscation and Machine Learing Based Analog Design," Drexel University, Philadelphia, Pennslyvania, March 2021 (online).

[13] Air Force Research Laboratory – Wright Patterson Air Force Base, "Progress Update – Temporal Circuit Obfuscation and Machine Learing Based Analog Design," Drexel University, Philadelphia, Pennslyvania, June 2020 (online).

[14] Bell Laboratory, "Heterogeneous Circuits: From On-chip Power Management to Security," Murray Hill, New Jersey, February 2020.

[15] IBM, "AFRL MINSAV ATC-DP Research and Academic Overview," Washington, D.C., November 2019

[16] Lockheed Martin, "IC Security Research Overview," Drexel University, Philadelphia, Pennslyvania, February 2018.

[17] BAE Systems, "Gate Level Logic Encryption for IC Security," teleconference with slides, July 2016.

[18] Raytheon, "Gate Level Logic Encryption for IC Security," teleconference with slides, July 2016.

[19] Sigenics Inc., "Gate Level Logic Encryption for IC Security," teleconference with slides, July 2016.

[20] Air Force Research Laboratory – Wright Patterson Air Force Base, "IC Security Research Overview," Drexel University, Philadelphia, Pennslyvania, July 2016.

[21] NXP Semiconductors, "Gate Level Logic Encryption for IC Security," teleconference with slides, June 2016.

[22] Altran, "Gate Level Logic Encryption for IC Security," teleconference with slides, June 2016.

[23] Trusted Semiconductor, "Gate Level Logic Encryption for IC Security," teleconference with slides, May 2016.

[24] Federal Reserve Bank of Philadelpiha, "Protecting Embedded Systems from Hardware Attacks," Drexel University, Philadelphia, Pennslyvania, February 2016.

[25] CEA Leti, " 3-D IC Research Overview," webinar, February 2016.

[26] Huawei Technologies, "Hardware Security and Trust," Drexel Univerisity, Philadelphia, Pennslyvania, December 2015.

[27] Lockheed Martin, "Overview of Current Research Activities," Drexel University, Philadelphia, Pennslyvania, May 2015.

[28] Lockheed Martin Teleconference, Drexel University, Philadelphia, Pennslyvania, March 2015.

[29] Lockheed Martin Mission Systems and Training (LMMST), Drexel University, Philadelphia, Pennslyvania, December 2014.

[30] Lockheed Martin Advanced Technology Laboratories (LMATL), Moorestown, New Jersey, July 2014.

[31] Qualcomm Research, University of Rochester, Rochester, New York, January 2012.

[32] Samsung Research., University of Rochester, Rochester, New York, September 2011.

[33] Kodak Research for supported projects, Kodak Park, Rochester, New York, bi-monthly from June 2009 to December 2011.

Grants

Written multiple grants for government granting agencies

- Office of Naval Research (ONR) and Department of Defense (DoD) Multidisciplinary University Research Initiative
- Air Force Research Laboratory
- National Science Foundation (NSF)
- Defense Advanced Research Projects Agency (DARPA)

Written multiple grants for industrial partnerships

- Cisco Systems, Inc. – Two projects awarded funding
- Tezzaron Semiconductor – DARPA sponsored fabrication run (3-D IC).
- Massachusetts Institute of Technology Lincoln Laboratory (MITLL) – DARPA sponsored fabrication run (3-D IC).
- Also submitted to Intel, Qualcomm, Semiconductor Research Corporation (SRC), and SEMATECH.

Awarded NSF/DoD/DoE Grants

1. Project Title: CAREER: Parameter Obfuscation: A Novel Methodology for the Protection of Analog Intellectual Property
   Proposal Number: 1751032
   Investigators: *Ioannis Savidis (PI*)
   Source of Support: National Science Foundation; Computer and Network Systems (CNS)
   Total Award Amount: $503,985
   Period Covered: 06/01/2018 – 05/31/2023
   Date Submitted: 07/19/2016
   Program Officer: Yan Solihin and Sandip Kundu
   Location of Project: Drexel University

2. Project Title: Security Through Obfuscation of Critical Analog Circuit Properties
   Proposal Number: N000382806
   Investigators: *Ioannis Savidis (PI*)
   Source of Support: Department of Energy – Honeywell FMT
   Total Award Amount: $94,000

Period Covered: 12/23/2020 – 06/30/2021
Date Submitted: 10/07/2020
Program Officer: Dan Ewing
Location of Project: Drexel University

3. Project Title: Temporal Circuit Obfuscation and Learning-based Automation of Analog and Mixed-signal Integrated Circuit Design
Proposal Number: FA8075-14-D-0025
Investigators: *Ioannis Savidis (PI*)
Source of Support: Air Force Research Laboratory
Total Award Amount: $170,731.00
Period Covered: 9/01/2019 – 11/30/2020
Date Submitted: 09/14/2018
Program Officer: Pompei Len Orlando
Location of Project: Drexel University

4. Project Title: Testbed for Experimental Validation of Security Techniques for the Protection of Circuit Integrity
Proposal Number: N00014-19-1-2396
Investigators: *Ioannis Savidis (PI*)
Source of Support: Office of Naval Research
Total Award Amount: $580,029.30
Period Covered: 06/01/2019 – 06/14/2020
Date Submitted: 07/06/2018
Program Officer: Sukarno Mertoguno
Location of Project: Drexel University

5. Project Title: Sequential Circuit Locking
Proposal Number: N000321940
Investigators: *Ioannis Savidis (PI*)
Source of Support: Department of Energy – Honeywell FMT
Total Award Amount: $49,999
Period Covered: 07/17/2019 – 11/31/2019
Date Submitted: 06/01/2019
Program Officer: Gabriel Luna
Location of Project: Drexel University

Awarded Student Fellowships

1. Student Name: Kyle Juretus
Advisor: Ioannis Savidis
Source of Support: National Defense Science and Engineering Graduate (NDSEG) Fellowship
Total Award Amount: $137,841 (stipend of $34,000 and tuition)
Period Covered: 09/01/2016 – 08/31/2019
Date Submitted: 12/18/2015
Location of Project: Drexel University

2. Student Name: Divy Pathak
Advisor: Ioannis Savidis
Source of Support: IEEE Circuits and Systems Sociey 2017 Pre-Doctoral Scholarship
Total Award Amount: $25,000 stipend
Period Covered: 07/01/2017 – 06/31/2018
Date Submitted: 02/15/2017
Location of Project: Drexel University

RESEARCH EXPERIENCE

- Designed and fabricated test circuits at IBM TJ Watson Research Center (Yorktown Heights, NY) characterizing the 3-D integration fabrication process (through-silicon via yield). Test circuits were also designed to electrically characterize the through-silicon via (TSV), investigate the impact of thermal cycling on the TSV, and examine mismatch losses (insertion, attenuation, reflection, transmission, and return) arising from TSV placement in high frequency signal paths.
- Electromagnetic modeling of the TSV for simulation in Ansoft (now part of Ansys) HFSS and Quick 3-D. Full wave simulations were performed to electrically characterize the TSV at IBM TJ Watson Research Center (Yorktown Heights, NY). Part of my research included tool development of a Java Script based GUI interface that automates model creation of TSV structures for HFSS and Quick 3-D simulation.
- System level design and implementation of a 3-D integrated intra-chip free-space optical interconnect system for multi-core communication with a group of five professors and twelve graduate students. Designed and fabricated photodetectors and VCSEL arrays, as well as a 3-D integrated transceiver and computing core. Included, additional test circuits investigating thermal conduction amongst 3-D stacked device planes and impact of on-chip decoupling capacitor placement on noise propagation.
- Developed closed-form expressions of the resistance, inductance, and capacitance of interplane 3-D vias.
- Designed a test chip to characterize ground and power noise on various 3-D power distribution topologies. The test chip was fabricated by MIT's Lincoln Laboratory (the 2nd test chip fabricated by MIT's Lincoln Labs).
- Electrically characterized the *RLC* impedance of interplane vias for 3-D integrated circuits; modeled 3-D via to 3-D via inductive and capacitive coupling noise for various circuit topologies.
- Designed circuitry to examine various clock and power distribution topologies for 3-D IC's with another student in a collaborative project with MIT's Lincoln Laboratory; clock distribution schemes implemented in silicon were H-tree, trunk, and ring; power was distributed through grid and periphery topologies.
- Implemented cosine transform function in hardware with team of three; developed schematics and layout for the ~38,000 transistor design using Mentor Graphic's ic and da programs; performed simulations to determine power consumption and overall functionality.
- Performed HSPICE simulations of both a 128x128 DRAM and SRAM cell with sense amplifier circuitry as part of two member group; analyzed power consumption and conducted transient analysis on both circuits.
- Designed (layout and schematic) and simulated a low-powered, pipelined 8-bit Brent-Kung adder in Cadence; performed simulations to determine the peak power consumption, set and hold times, and functionality with transient analysis.
- Designed the phase detector, charge pump, and loop filter of an injection-locked oscillator that included a front end of a receiver with ADS; performed simulations on each block of the design to assure each block met specifications set at the onset of the project.
- Examined low power clock distribution networks through a literature search; focused on identifying means of minimizing power consumption on the clock distribution network; presented results to class.
- Modified the Calibre LVS deck to detect devices not currently included such as via chains and kelvins; developed a general MOSFET definition to detect layers overlaying transistors; combined LVS decks for cmos090nvm, cmos090soi, and cmos090 into a single deck (while at Freescale).

PROFESSIONAL EXPERIENCE

September 2019 – present: **Associate Professor, Drexel University**, *Philadelphia, PA*

Director, *Integrated Circuits and Electronics (ICE) Design and Analysis Laboratory*

Security-aware integrated circuit design, specifically obfuscation for digital and analog circuits

Ultra low-power sub/near-threshold circuit techniques and methodologies

3-D and 2.5D heterogeneous integrated circuits – power and clock delivery, thermal characterization and management

Workload-aware SMART on-chip power management.

August 2013 – August 2019: **Assistant Professor, Drexel University**, *Philadelphia, PA*

Director, *Integrated Circuits and Electronics (ICE) Design and Analysis Laboratory*

Security-aware integrated circuit design, specifically obfuscation for digital and analog circuits

Ultra low-power sub/near-threshold circuit techniques and methodologies

3-D and 2.5D heterogeneous integrated circuits – power and clock delivery, thermal characterization and management

Workload-aware SMART on-chip power management.

May 2009 – June 2011: **IBM Research**, *Yorktown Heights, NY*

Manager: Dr. John U. Knickerbocker, *Mentors*: Dr. Bucknell C. Webb, Dr. Bing Dang, Mr. Paul S. Andry

Group: System on Package and 3-D Integration

Designed circuits to examine package level integration (die on silicon carrier technology that includes a redistribution level for die to die bi-directional communication) through various test vehicles that include C4 bump chains, interdie C4 bump chains, four-point measurements for C4 bump characterization, 20 to 40 mm long transmission lines, and mechanical tests to determine the minimum spacing permitted between to die bonded to the same silicon carrier.

Designed mask sets characterizing the electrical properties of 3-D vias and microbumps. Designed multi-voltage tap structures (on-chip four point measurements), TSV via chains, connectivity test sites, and other test vehicles to characterize the TSVs.

Analyzed DRC, LVS, extraction, and Router tools for potential use in 3-D design flow.

Improved GUI and continued high frequency electrical characterization and modeling of interplane 3-D vias using Ansoft's Quick 3-D and HFSS.

May 2008 – August 2008: **IBM Research**, *Yorktown Heights, NY*

Manager: Dr. John U. Knickerbocker, *Mentor*: Dr. Chirag Patel

Group: System on Package and 3-D Integration

Completed high frequency electrical characterization and modeling of TSVs using Ansoft's Quick 3-D and HFSS.

Developed Java interface with Quick 3-D and HFSS to quickly produce models of TSV's for various lengths, diameters, dielectric thickness, via-to-via pitch, and number of surrounding vias for electrical simulation.

May 2007 – August 2007: **Freescale Semiconductor**, *Austin, TX*

Manager: Dr. Robert E. Jones, *Mentor:* Dr. Ankur Jain, Dr. Ritwik Chatterjee, Dr. Syed M. Alam

Group: System Interconnect Solutions and 3-D Integration

Performed electrical characterization and modeling of interplane 3-D vias.

System level HSPICE simulations of global interconnects for both 2-D and 3-D chip configurations.

May 2006 – August 2006: **Freescale Semiconductor**, *Austin, TX*

Manager: Dr. Brad Smith, *Mentor:* Dr. Douglas Reber

Group: Technology Validation

Modified the Calibre LVS deck to detect via chains and kelvins (modifying SVRF scripts).

Added general MOSFET definition to Calibre LVS deck (with SVRF language).

Combined cmos090nvm, cmos090soi, and cmos090 into a single LVS deck.

September 2007 – August 2013: **University of Rochester Graduate Research Assistant (RA)**, *Rochester, NY*

Advised by: Prof. Eby G. Friedman

Member of the *High Performance Integrated Circuit (HPIC) Design* Laboratory

Experimentally quantified noise propagation in 3-D integrated circuits with respect to 3-D power distribution network topology

Examined various clock and power distribution schemes for 3D-IC's; MIT Lincoln Laboratory fabricated test circuits in 2007 and 2010.

Performed *RLC* modeling and characterization of 3D vias and signal integrity simulations for MIT Lincoln

Laboratory's 3D-IC process.

January 2006 – June 2006: **University of Rochester Graduate Research Assistant (RA)**, *Rochester, NY*

Advised by: Profs. Martin Margala and Marc J. Feldman

Developed a 1 T-Hz ballistic deflection transistor.

Fabricated ballistic deflection transistor at Cornell University's NanoScale Science and Technology Facility (CNF).

January 2004 – May 2005: **Duke University Pratt Fellowship,** *Undergraduate Academic Researcher*

Advised by: Prof. Patrick Wolf

Enhanced Backpack Design for Brain Machine Interface. Programmed an Elf3 ultra low power XScale PXA255 in VHDL to control the electrical frontend of the Brain Machine Interface, where the Brain Machine Interface is connected to the brain of a rhesus monkey.

May 2003 – August 2003: **University of Rochester's Laboratory for Laser Energetics***, Undergraduate Researcher*

Advised by: Prof. Roman Sobolewski

Developed magnetic susceptibility experiment to examine transition temperatures of very small (few mm in length and width) single crystal superconducting material.

May 2002 – August 2002: **University of Rochester's Laboratory for Laser Energetics***, Undergraduate Lab Technician*

Advised by: Prof. Roman Sobolewski

Developed functional schematic of Omega EP laser system including beamlines, mirrors, actuators, amplifiers, compression chamber, and target chamber.

June 2000 – August 2000: **University of Rochester's Laboratory for Laser Energetics***, Academic Researcher*

Advised by: Prof. Roman Sobolewski

Selected as one of 15 (from 80 applicants) high school students to participate in the Summer Research Program. Examined Josephson Junctions using JSPICE simulations and lab experimentation.

PROFESSIONAL MEMBERSHIPS

Institute of Electrical and Electronics Engineers (IEEE) – member since 2004, Senior member since October 2018

- Member of Circuits and Systems Society, Solid-State Circuits Society, Microwave Theory and Techniques Society, and Electron Devices Society
- Member of Council on Electronic Design and Automation (CEDA)

Association of Computing Machinery (ACM) – member since 2014

Optical Society of America (OSA) – member March 2012 to August 2017

American Society for Engineering Education (ASEE) – member since July 2012

National Science Teachers Association (NSTA) – member June 2012 to June 2019

PROFESSIONAL SERVICE

Associate Editor

IEEE Transactions on Very Large Scale Integration Circuits (TVLSI) – 2013-present

Microelectronics Journal (MEJ) – 2013-present

Journal of Circuits, Systems, and Computers (JCSC) – 2013-present

Organzing Committee Member

Finance Chair, *IEEE International Symposium on Circuits and Systems (ISCAS)* – 2022

Program Chair, *IEEE/ACM Great Lakes Symposium on Very Large Scale Integration (GLSVLSI) - 2021*

Finance Chair, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST) – 2021*

Program Chair (Security-1 Research Topic), *IEEE/ACM Design Automation Conference (DAC)* - 2021

Registration Chair, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST) – 2020*

Finance Co-Chair, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST) – 2020*

Registration Chair, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST) – 2019*

Publications Chair, *IEEE/ACM Great Lakes Symposium on Very Large Scale Integration (GLSVLSI) – 2019*

Panel Chair, *IEEE/ACM Great Lakes Symposium on Very Large Scale Integration (GLSVLSI) – 2018*

Registration Chair, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST) – 2018*

Registration Chair, *IEEE International Verification and Security Workshop (IVSW) – 2018*

Registration Chair, *IEEE International Symposium on Hardware Oriented Security and Trust (HOST) – 2017*

Registration Chair, *IEEE International Verification and Security Workshop (IVSW) – 2017*

Publicity Chair, *IEEE/ACM System Level Interconnect Prediction (SLIP) Workshop – 2016*

Technical Program Committee Member

IEEE /ACM International Conference on Computer-Aided Design (ICCAD) – 2017, 2018

IEEE /ACM Design Automation Conference (DAC) – 2019, 2020

IEEE /ACM International Conference on Computer Design (ICCD) – 2019, 2021

IEEE International Symposium on Hardware Oriented Security and Trust (HOST) – 2016, 2017, 2018, 2020, 2021

IEEE/ACM Great Lakes Symposium on Very Large Scale Integration (GLSVLSI) – 2015, 2016, 2017, 2018, 2019, 2020, 2021

IEEE International Symposium on Circuits and Systems (ISCAS) – 2014, 2015, 2016, 2017, 2018, 2019, 2020, 2021

IEEE International Symposium on VLSI (ISVLSI) – 2020, 2021

IEEE/ACM System Level Interconnect Prediction (SLIP) Workshop – 2016, 2017, 2018, 2019

IEEE International Symposium on Quality Electronic Design (ISQED) – 2020, 2021

IEEE International Conference on Omni-Layer Intelligent Systems (COINS) – 2020

IEEE Circuits and Systems (CAS) Society VLSI Systems and Applications Technical Committee (VSA-TC) – member since 2017

External reviewer for

Journals

IEEE Transactions on Very Large Scale Integration (VLSI) Circuits (TVLSI); IEEE Transactions on Electron Devices (TED); IEEE Transactions on Circuits and Systems-II (TCAS-II); IEEE Transactions on Computer-Aided Design (TCAD); IEEE Transactions on Electron Device Letters (TEDL); ASP Journal of Low Power Electronics (JOLPE); Analog Integrated Circuits and Signal Processing (ALOG); Microelectronics Journal; IEEE Transactions on Advanced Packaging (TADVP); IEEE Transactions on Components, Packaging and Manufacturing Technology (TCPMT); IEEE Transactions on Computers (TC); ACM Journal on Emerging Technologies in Computing Systems (JETCS)

Conferences

Design, Automation, and Test in Europe (DATE); International Symposium on Circuits and Systems (ISCAS); International Conference on Computer Design (ICCD); System-on-Chip Conference (SoCC); Asia Pacific Conference on Circuits and Systems (APCCAS); International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS); International Symposium on Networks-on-Chip (NoCS); Great Lakes Symposium on VLSI (GLSVLSI); International Conference on Omni-Layer Intelligent Systems (COINS)

Duke University Alumni interview program – Interviewed over 15 potential undergraduate candidates for admittance to Duke since Spring 2007.

University of Rochester GEAR program interviewer – Interviewed 8 students for prestigious 5 year B.S/M.S. program with tuition waver – Spring 2009 and 2010.

Volunteer for the Finger Lakes FIRST (For Inspiration and Recognition of Science and Technology) LEGO League Tournament since December 2008.

IEEE graduate president – University of Rochester, Fall 2006- Spring 2007.

Hosted guest lecturer from IBM Research, Yorktown Heights, NY on January 2007 – Dr. Barry Rubin presented a seminar and workshop on a full wave electromagnetic toolset developed by IBM. I was his guide around the university and department, setup the projector for his presentation, reserved the appropriate rooms for the seminar and workshop, and was the intermediary for any questions about the tool prior to and after Dr. Rubin's visit.

IEEE undergraduate secretary student body board member – Duke University, 2004-2005.

TEACHING

Academic Experience

September 2013 – Current : Drexel University, *Philadelphia, PA*

Primary instructor of developed undergraduate and graduate course on hardware security: *Hardware Security & Trust* (ECE-C 476)

Primary instructor of developed undergraduate and graduate crosslisted course sequence on VLSI: *Introduction to VLSI Design* (ECE-C 471/571), *Custom VLSI Design and Analysis I* (ECE-C 472/572), and *Custom VLSI Design and Analysis II* (ECE-C 473/573). Developed course material, laboratory assignments, mid-term and final examinations, and quarter long IC design projects.

Primary instructor for undergraduate electrical and computer engineering course: *Digital Logic Design* (ECE 200)

Instructor for introductory freshman course: *Computation Lab I* (ENGR 121). Over 900 students of mostly freshmen across the College of Engineering are introduced to computation through Matlab.

September 2011 – May 2012 : University of Rochester Kearn Center Tutor, *Rochester, NY*

One on one tutoring of under-represented minorities in *Calculus* (MTH 141) and *Introduction to Signals and Circuits* (ECE 111) through the Kearn Center (mission to provide education opportunities and assistance for low-income, first-generation college, and underrepresented minority students).

September 2005 – May 2007 : University of Rochester Teaching Assistant (TA), [Rochester, NY]

Prepared, organized, and guided students through lab exercises and course material for *Logic Design* (ECE 112L, undergraduate logic design), *Circuits and Microcontrollers for Scientists and Engineers* (ECE 210L, undergraduate class), and *Performance Issues in IC/VLSI Design and Analysis* (ECE 465, graduate class). Held one-on-one office hours, group based learning sessions, laboratory assistance, and recitations.

Member of Teaching Organizations

American Society for Engineering Education

National Science Teachers Association

The Chronicle of Higher Education

SKILLS AND HOBBIES

Computer

Computer Languages: Assembly (MIPS, Intel x86), VHDL, Verilog, C++/C, Java, SVRF scripting language, Perl TVF, and Tcl/Tk.

Networking programs: Tera Term, WS_FTP, SSH Client.

Competency in: Sun (Unix), Apple (MacOS), and PCs (Windows/Linux).

Proficiency with: Pspice, Jspice, Hspice, Latex, Maple, Matlab, Powerview, LabVIEW, Max + Plus II, Espresso, Mathematica, Mentor Graphics (ic & da), Cadence (Virtuoso , Assura, Analog Environment, & Encounter), CalibreDRV, Agilient ADS, Quicksim, Asitic, Comsol Multiphysics, Ansoft (Quick 3-D & HFSS).

Lab equipment

Agilent E8364A 45 MHz to 50 GHz PNA series network analyzer

HP 54750A digitizing oscilloscope

HP 4145B semiconductor parameter analyzer

Agilent 8565E spectrum analyzer

West-Bond 7400 ultrasonic, thermosonic, and thermocompression wire bonding methods

REFERENCES

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